AMENDMENTS TO THE CLAIMS

The listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Canceled)

2. (Previously Presented) A method comprising:

storing data from a primary and a secondary source into a primary memory and a secondary memory based on a primary clock signal and a secondary clock signal;

framing data being outputted from the primary and the secondary memory; and

adjusting the primary clock signal to adjust an occupancy of the primary memory.

3. (Previously Presented) The method of claim 2, further comprising:

generating a signal indicating that a phase adjustment of the primary clock signal is needed.

4. (Previously Presented) The method of claim 2, further comprising:

calibrating a phase adjuster for the primary clock signal.

5. (Previously Presented) The method of claim 2, further comprising:

calculating a delay for the primary clock signal to adjust the primary clock signal to accelerate or decelerate the framing of data in the primary memory.

6. (Previously Presented) The method of claim 2, wherein the primary memory is a memory that is currently in use for transmitting a frame, and

wherein the secondary memory is a memory that is not in use for transmitting a frame.

7. (Previously Presented) The method of claim 2, further comprising:

adjusting the primary clock signal to adjust the occupancy of an egress memory.

8. (Previously Presented) A device comprising:

a primary memory;

a secondary memory; and

a clock control logic circuit coupled to the primary memory and secondary memory to adjust a primary clock signal to synchronize an occupancy of the primary memory and the secondary memory.

9. (Previously Presented) The device of claim 8, further comprising:

a primary deframer coupled to the primary memory; and

a secondary deframer coupled to the secondary memory.

10. (Previously Presented) The device of claim 8, wherein the clock control logic comprises:

a phase adjuster;

cycle control logic coupled to the phase adjuster; and

step pulse generator logic coupled to the cycle control logic.

11. (Previously Presented) The device of claim 10, wherein the phase adjuster comprises:

a set of delay cells to alter the phase of a primary clock signal.

12. (Previously Presented) An apparatus comprising:

a primary control card;

a secondary control card; and

a traffic card coupled to the primary control card and secondary control card, the traffic card having a clock control logic circuit coupled to a primary memory and secondary memory to

adjust a primary clock signal to synchronize an occupancy of the primary memory and the secondary memory.

13. (Previously Presented) The apparatus of claim 12, wherein the primary control card is in use and the secondary control card is a back up card.

14. (Previously Presented) The device of claim 12, further comprising:

a second traffic card coupled to the primary control card and the secondary control card.

15. (Previously Presented) The device of claim 12, wherein the clock control logic comprises:

a phase adjuster;

cycle control logic coupled to the phase adjuster; and

step pulse generator logic coupled to the cycle control logic.

16. (Previously Presented) An apparatus comprising:

means for storing data from a primary and a secondary source into a primary memory and a secondary memory based on a primary clock signal and a secondary clock signal;

means for framing data being outputted from the primary and the secondary memory; and

means for adjusting the primary clock signal to adjust an occupancy of the primary memory.

17. (Previously Presented) The apparatus of claim 16, further comprising:

means for generating a signal indicating that a phase adjustment of the primary clock signal is needed.

18. (Previously Presented) The apparatus of claim 16, further comprising:

means for calibrating a phase adjuster for the primary clock signal.

19. (Previously Presented) The method of claim 16, further comprising:

means for calculating a delay for the primary clock signal to adjust the primary clock signal to accelerate or decelerate the framing of data in the primary memory.

20. (Previously Presented) The method of 16, further comprising:

means for adjusting the primary clock signal to adjust an occupancy of an egress memory.

21. (Previously Presented) A machine readable medium, having instruction stored therein, which when executed cause a computer to perform a set of operations comprising:

storing data from a primary and a secondary source into a primary memory and a secondary memory based on a primary clock signal and a secondary clock signal;

framing data being outputted from the primary and the secondary memory; and

adjusting the primary clock signal to adjust an occupancy of the primary memory.

22. (Previously Presented) The machine readable medium of claim 21, having further instructions stored therein, which when executed cause a computer to perform a set of operations comprising:

generating a signal indicating that a phase adjustment of the primary clock signal is needed.

23. (Previously Presented) The machine readable medium of claim 21, having further instructions stored therein, which when executed cause a computer to perform a set of operations comprising:

calibrating a phase adjuster for the primary clock signal.

24. (Previously Presented) The machine readable medium of claim 21, having further instructions stored therein, which when executed cause a computer to perform a set of operations comprising:

calculating the delay for the primary clock signal to adjust the primary clock signal to accelerate or decelerate the framing of data in the primary memory.

25. (Previously Presented) The machine readable medium of claim 21, wherein the primary memory is a memory that is currently in use for transmitting a frame, and

wherein the secondary memory is a memory that is not in use for transmitting a frame.

26. (New) An apparatus comprising:

a traffic card including,

a first and second ingress FIFO to be coupled to respectively receive both data and a clock signal from a first and second control card;

a first and second deframer respectively coupled to said first and second ingress FIFOs;

an aligner coupled to said first and second FIFO to keep the occupancy of data therein in sync based upon detected differences in alignment of data being received by the first and second deframers;

a clock control logic to receive the clock signal from each of said first and second control cards, to exchange with a PLL a first clock signal for a PLL adjusted clock signal, and to provide said PLL adjusted clock signal to said aligner, said first ingress FIFO, and said second ingress FIFO, said clock control logic including,

a phase adjuster to provide said first clock signal based on a currently selected one of the clock signals from said first and second control cards.